

WHAT IS CLAIMED

1. An amplifier architecture comprising:

an input port to which a signal to be amplified is coupled;

5 an output port from which an amplified signal is derived;

10 a first amplification path coupled between said input port and said output port and including a first gain stage and an output transistor having a control input terminal coupled to said first gain stage and an output terminal coupled to said output port, said first amplification path being operative to compensate for an offset voltage component in said amplified signal associated with said output transistor;

15 a second amplification path coupled between said input port and said output port and being operative to correct for long term drift errors in said main amplification path; and

20 a third amplification path coupled between said input port and said output port and being operative to correct for high frequency transient effects in said main amplification path.

2. The amplifier architecture according to claim 1, wherein said output transistor comprises a source follower-configured field effect transistor.

3. The amplifier architecture according to claim 2, wherein said first amplification path is operative to compensate for a gate-to-source voltage offset component in said amplified signal associated with said field effect transistor.

4. The amplifier architecture according to claim 1, wherein said first amplification path includes a positive feedback loop coupled between said output transistor and said input port, and being operative to feed back a voltage representative of said offset voltage to said input port, so as to be combined with said signal to be amplified and applied to said first gain stage.

5. The amplifier architecture according to claim 4, wherein said second amplification path includes a negative feedback loop coupled between said output port and said input port, and being operative to feed back said amplified signal to said input port, so as to be combined with said signal to be amplified and being applied to a second gain stage, said second gain stage having an output thereof combined with the output of said first gain stage for application to said control 10 electrode of said transistor.

6. The amplifier architecture according to claim 5, wherein said third amplification path includes a fast path coupled between said input port and said output

port, and being operative to amplify said input signal 5 by way of a third gain stage, said third gain stage having an output thereof coupled to said output port, so as to be combined with signals amplified by said first and second gain stages and provided at said output terminal of said output transistor.

7. The amplifier architecture according to claim 8, wherein said third amplification path has a bandwidth that overlaps the bandwidth of said first amplification path.

8. The amplifier architecture according to claim 7, wherein said second amplification loop has a bandwidth on the order of decade lower than bandwidths of said first and third amplification loops.

9. An amplifier architecture comprising:
an input port to which a signal to be amplified is coupled;
an output port from which an amplified signal is 5 derived;
a first amplification path coupled between said input port and said output port and including a first gain stage;
an output transistor coupled in voltage follower 10 configuration having a control terminal coupled to said first gain stage and an output terminal coupled to said output port;

15 a first, positive feedback compensation loop, coupled between said output transistor and said input port, and being operative to feed back a voltage representative of an offset voltage between said control terminal and said output terminal to said input port, so as to be combined with said signal to be amplified and applied to said first gain stage, and compensate for 20 said offset voltage in said amplified signal;

25 a second, negative feedback loop, coupled between said output port and said input port, and being operative to feed back said amplified signal to said input port, so as to be combined with said signal to be amplified and being applied to a second gain stage, said second gain stage having an output thereof combined with the output of said first gain stage for application to said control electrode of said transistor; and

30 a third, fast path utilizing negative feedback coupled between said input port and said output port, and being operative to amplify said input signal by way of a third gain stage, said third gain stage having an output thereof coupled to said output port, so as to be combined with signals amplified by said first and second 35 gain stages and provided at said output terminal of said output transistor.

10. The amplifier architecture according to claim 9, wherein said output transistor comprises a source follower-configured field effect transistor.

11. The amplifier architecture according to claim 10, wherein said first, positive feedback loop is operative to compensate for a gate-to-source voltage offset component in said amplified signal associated 5 with said field effect transistor.

12. The amplifier architecture according to claim 9, wherein said third loop has a bandwidth that overlaps the bandwidth of said first loop.

13. The amplifier architecture according to claim 9, wherein said second, negative feedback loop has a bandwidth on the order of decade lower than bandwidths of said first and third loops.

14. A method of controlling the operation of a voltage follower-configured output transistor having a control electrode thereof coupled to receive a signal to be amplified thereby and an output electrode thereof 5 providing an amplified signal, said method comprising the steps of:

(a) coupling a signal to be amplified to a first gain stage an output of which is coupled to said control electrode;

10 (b) combining a voltage representative of an offset voltage between said control electrode and said output electrode with said signal to be amplified so as to compensate for said offset voltage in said amplified signal;

15 (c) differentially combining said amplified signal with said signal to be amplified via a second gain stage to produce a difference signal and coupling said difference signal with the output of said first gain stage for application to said control electrode of said 20 transistor; and

(d) coupling said signal to be amplified to a third gain stage an output of which is coupled to said output port and combined thereby with said amplified signal.

15. The method according to claim 14, wherein said output transistor comprises a source follower-configured field effect transistor.

16. The method according to claim 14, wherein said second gain stage has a bandwidth on the order of decade lower than bandwidths of said first and third gain stages.

17. The method according to claim 14, wherein said third gain stage has a bandwidth that overlaps the bandwidth of said first gain stage.

18. The method according to claim 14, wherein said third gain stage provides for instantaneous correction at the combined output of step (d).